Andrew W. Moore
University of Cambridge
Systems Research Group

Has: Lots making networks work
A love of measuring stuff
Proving hardware is not hard
Wants: things to measure and
to understand performance
& how/where to make
changes that matter most

Ahmed Al-Quzweeni – PhD student

University of Leeds

School of Electronic and Electrical Engineering / ICaPNet

Had: Installed and run 3G MSC, SMS, IN, and PSTN.

been lecturing at cisco netacad (Al-Mansour Academy)

Want: to get start with netFPGA

to get start with embedded systems

Believe: “That which can be asserted without evidence, can be dismissed without evidence”

Dipartimento di Ingegneria e Scienze dell'Informazione e Matematica

Università degli Studi dell'Aquila

INCIPICT
Innovating City Planning through Information & Communications Technologies

Andrea Marotta

Ph.D. Student

Department of Information Engineering, Computer Science and Mathematics at University of L'Aquila, Italy

e-mail: andrea.marotta@graduate.univaq.it
Skype: andreamarotta.skype

Research Interests

5G Radio Access Network Design, Optical Networking for 5G, PON Backhauling, PON Fronthauling, RAN Functions Placement

- Our effort is to green the Internet by providing energy efficient data center networks through optical interconnectivity inside data centers using optical components.

- Our research focuses on designing new optical data center architectures, where the NetFPGA is developed as high speed customizable network interface card.

- Attending this Summit will help answer several questions and solve some obstacles we faced while developing the NetFPGA.

Azza Elterifi

scaeae@leeds.ac.uk

Institute of Communication and Power Networks (ICaPNet)

University of Leeds

Cathal McCabe

- Xilinx University Program EMEA
  - Xilinx Ireland, Dublin
- Senior Applications Engineer
  - Responsible for XUP partnerships in EMEA including NetFPGA
  - XUP trainer
    - Vivado, HLS, Zynq, series 7 devices
  - PYNQ (Python on Zynq) developer
- Contact me about
  - XUP NetFPGA donations, academic pricing for boards, Vivado, 10G licensing etc
- cathal.mccabe@xilinx.com

XILINX
UNIVERSITY PROGRAM

Daniele Moro

POLITECNICO
MILANO 1863

- MSc Student in Telecommunication Engineering

- Interested in:
  - Software-Defined Networking stateful data planes
  - Tasks offloading to stateful data planes
  - Learning how the things work!

- I want to learn as much as possible on NetFPGA (NO exerperience)

daniele1.moro@mail.polimi.it

David Lake

- Part-time PhD student @ UofSurrey/5GIC:
  - Interest in 5G Packet Core (“Evolved” EPC?!) ‘cos new AI in 5G alone ≠ IMT-2020
  - Thinking about ideal hardware/software split in Virtualisation
  - Trying not to ride the “Hey Guys – let’s virutalise everything because virtual = GOOD” band-wagon
  - Support new protocols

- Day-job (?) – SP Solutions Architect @ DELL/EMC
  - Past; Mobility CTO group @ Cisco

- Want to understand scope/uses of NetFPGA

- Want to complete my PhD before I’m even older…

d.lake@surrey.ac.uk

Davide Sanvito

Politecnico di Milano
Advanced Network Technologies LABoratory

- Research interests in:
  - Software-Defined Networking Stateful Dataplanes
  - Traffic Engineering in Software-Defined Networking

- Want to learn about NetFPGA and its community

davide.sanvito@polimi.it

Diana Andreea Popescu
PhD Student
Marie Curie Early-Stage Researcher
System Research Group
University of Cambridge

UNIVERSITY OF CAMBRIDGE

Research interests:

- Network Latency Measurements
- Network Latency Impact on Cloud-based Application Performance
- SDN and Programmable Data Planes
- Working in the Marie Curie ITN METRICS project

NetFPGA Developers Summit 2017

Name:

- Dixon Salcedo

Education:

- PhD. Universidad Pontificia Bolivariana. Medellín (Colombia). 2014 - (expected).
- MSc in Free Software. Universidad Autónoma de Bucaramanga, Bucaramanga (Colombia) 2011.
- Undergraduate Degree in Engineering Systems. Universidad Autónoma del Caribe, Barranquilla (Colombia) 2003.

Position:

- Assistant Professor at the Department of Computer Science and Electronics, Universidad de la Costa, Barranquilla, Colombia, since 2011.

George Zervas

Gianni Antichi

Senior Research Associate
System Research Group
University of Cambridge

UNIVERSITY OF CAMBRIDGE

- SDN network architectures (**TouSIX, ENDEAVOUR**)
- Network Systems Performance characterization (**OSNT**, **OFLOPS-Turbo**, **pciebench**)
- Packet classification (**Classbench-ng**)

- Measurement-informed network management

  Can we improve network management with advanced SDN-inspired measurements?

OSNT: OPEN SOURCE NETWORK TESTER

OSNT: Open Source Network Tester

ENDEAVOUR

ENDEAVOUR: towards a flexible software-defined network ecosystem

SSICLOPS
Secure and Scalable Infrastructures for Cloud Operators

SSICLOPS: Scalable and Secure Infrastructure for Cloud Operations

NetFPGA

Università
della
Svizzera
italiana

Huynh Tu Dang
huynh.tu.dang@usi.ch
PhD Candidate @ USI Lugano, Switzerland

Research interests

- Software-defined networking
- Reliable distributed systems

Current projects

- NetPaxos
- P4Benchmark Suite

What to expect at NetFPGA Summit?

- Getting started with NetFPGA
- Know what are other people doing
- Possibly contributing to P4FPGA compiler

Jan Kučera

BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF INFORMATION TECHNOLOGY

Ph.D. student @ FIT BUT

- Packet classification in high-speed networks
- Visitor @ CL, P4 for network monitoring

Researcher @ CESNET

CESNET

liberouter

- 27 academic institutions
- Czech NREN, ~ 400 000 users
- FPGA-based NICs, COMBO, NetCOPE
- Software Defined Monitoring
- DDoS Protector

UNIVERSITY OF CAMBRIDGE

Background & skills:

- ✓ Hardware design
- ✓ Fibre optics
- ✓ Coding theorem

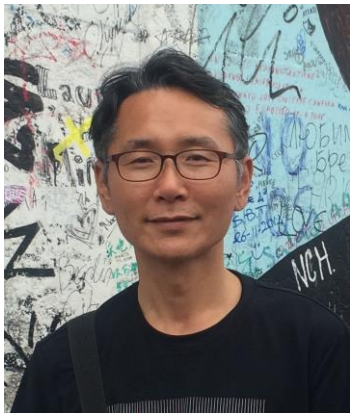
Research Interest:

- ➢ Physical Layer Architecture
- ➢ Multiple input Multiple output optics
- ➢ Forward Error Correction

NetFPGA:

- ➢ Joined just before SUME release
- ➢ Eth-DDAS project
- ➢ Ongoing >>> Embedded MIMO channel modelling

Jingyun Zhang
3rd year PhD student
jz377@cam.ac.uk



Who am I ?

My name is Jong Hun Han and I'm Research Associate working at NetOS group within the Computer Laboratory.

What do I do?

I'm currently working on a project, Endeavour: Towards a flexible software-defined network ecosystem, funded from EU Horizon 2020 program. I'm porting the OSNT project to the NetFPGA-SUME platform.

What am I interested in?

I'm mostly working on the NetFPGA platform and interested in implementing network hardware like NIC, Switch, and CPU as well. I have implemented Blueswitch and integrated MIPS and RISC-V processors on the NetFPGA platforms.

Jose Fernando Zazo

- **PhD Student** at the **Autonomous University of Madrid**, Spain
- Full-time **employee at Naudit HPCN**, a startup in the telecommunications sector, oriented to the analysis of multigigabit network infrastructures
- Recent work and topics of interests:
  - Open source DMA core with SRIOV capabilities
  - Traffic player at 100 Gbps
  - Application of hardware accelerators for traffic filtering and the inspection of the payload of the packets

josefernando.zazo@naudit.es

naudit High Performance Computing and Networking

HPCN High Performance Computing and Networking

UAM UNIVERSIDAD AUTÓNOMA DE MADRID

T. Khoa Phan

- **Research associate - University College London, UK (2014 – present)**
  - Multicast protocol for streaming systems, software defined networking (SDN), cloud and edge cloud computing, P4/NetFPGA.
  - Projects: EU CHIST-ERA CONCERT (2014 – 2018), H2020 5G-MEDIA (2017 – 2020), FP7 FUSION (2013 – 2016).
- **M.Sc. and PhD – INRIA Sophia Antipolis, France (2010 –2014)**
  - Green networking, operations research, TCP congestion control.
- **My talk:** "*Optimising streaming systems with SDN/P4/NetFPGA*"

Research Interests:

Network protocol design,
Energy efficiency in optical access networks
5G Fronthaul and Backhaul interfaces
5G Convergence, and flexible architectures using SDN solutions

Koteswararao Kondepu
Senior Research Associate
koteswararao.kondepu@gmail.com

highperformancenetworks group

5G PPP

5G-XHaul

University of BRISTOL

Liselot de Jonge

Marcin Wójcik

Research Associate
Systems Research Group
Networks and Operating Systems group

UNIVERSITY OF CAMBRIDGE

SSICLOPS

Emu

NetFPGA

Research interests and ongoing work:

- Efficient and secure implementations of cryptographic algorithms and network protocols (mostly in hardware)
- Performance characterisation of network components
- Novel protocol implementations in NetFPGA-based switches
- High-speed DMA for NetFPGA-based NIC

* SSICLOPS: Scalable and Secure Infrastructure for Cloud Operations

Marco Spaziani Brunella

Junior Research Associate
Networking Group
University of Rome Tor Vergata

- Digital Systems Design and Arithmetic (particular emphasis on CPU architecture)
- Software Defined Networking
- SoC Development

Neelakandan Manihatty Bojan (Neels)

Bio:

- 3rd year PhD student at Computer lab, Cambridge
- Working on Schedulers for hybrid data center networks.

Research Interests:

- Reconfigurable computing
- Data center networks
- optical networks
- Hybrid networks

Talk to me about:

- Hardware design
- Data center networks
- Switching architectures

Neelakandan Manihatty Bojan (Neels)
3rd year PhD student
nm525@cl.cam.ac.uk

Pietro Giuseppe Bressana

Università della Svizzera italiana

Education:

- [2016] PhD Candidate in Computer Science
  USI Lugano (Switzerland)

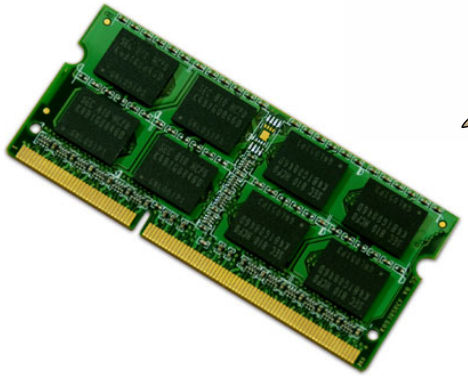
- [2015] Master's degree in Computer Engineering
  Politecnico di Milano (Italy)

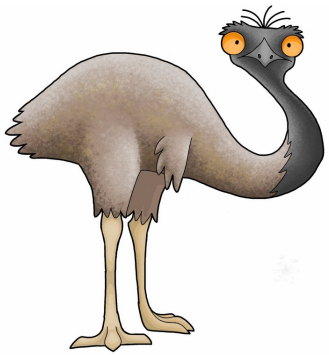
Research field:

- FPGA architectures in the networking domain
- FPGA architectures for high performance computing

Developers Summit:

- Emu project
- Contributing to the NetFPGA Sume architecture





Renier Eijkelestam

RICARDO SANTOS

- PhD student in Karlstad University, Sweden since 2016
- Research interests:
  - Software-defined Networks
  - Multi-path transport protocols
  - Wireless Backhaul Management
  - Programmable data planes

COMPUTER SCIENCE
DATAVETENSKAP

Salvator Galea

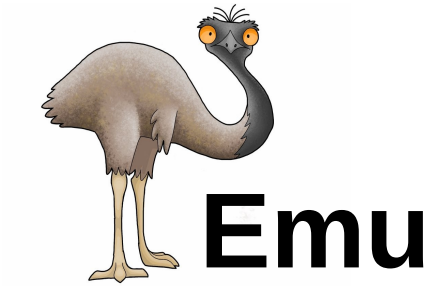
Research Assistant
Systems Research Group
Networks and Operating Systems group

UNIVERSITY OF CAMBRIDGE

My work focus on:

NetFPGA

- Support the NetFPGA platform & community
- Maintain the NetFPGA-SUME code-base & infrastructure



Emu

- Execution of high-level descriptions of network services, written in C#, on the NetFPGA-SUME
- Library that maps programming and networking abstractions to bus protocols, memory interfaces, and basic frame-handling functionalities
- Reference designs

Sanaa Hamid Mohamed,
University of Leeds,
Institute of Communication and Power Networks

Interested in enhancing data center networking for big data applications.

Looking forward to learn more about NetFPGA to achieve better data centers networking.

Seokwon Jang
Korea University
School of Electrical Engineering

What I have

- Experience in control plane architecture design

What I want (**A novice researcher in data plane**)

- To understand what FPGA is and how I can programming my program in netFPGA platform

- **Sol Han**
- School of Electrical engineering
- Mobile network and communication lab.
- E-mail address : losbiss@gmail.com
- Interested in SDN and programmable data plane
- I want to learn how to use P4->NetFPGA in this summit

Stephen Ibanez

- 2nd year PhD Candidate at Stanford in EE
- Advisor: Nick McKeown
- Working closely with Gordon Brebner (Xilinx Labs)
- Research Interests
  - Programmable networking
  - Network testing / verification
  - Computer / network security
- Current Projects
  - P4-NetFPGA
- Potential Future Projects
  - P4 workflow for OSNT
  - Programmable scheduling on NetFPGA

Taylan Özgür Toygarlar, IMC Financial Markets

Taylan is a technologist holding a researcher position in IMC Financial Markets, currently focusing on future technologies and products for trading the markets more efficiently. He holds a B.Sc. in Electrical and Electronics Engineer from METU, and an M.Sc. on Computer Science from RWTH-Aachen. His research covers a broad range from computer architecture to machine learning, with a strong focus on delivering production quality prototypes. Prior to IMC Financial Markets, he was part of the scientific staff in University of Amsterdam, Intelligent Systems Lab, working at the intersection of academia and industry, on image and video recognition. Within IMC, he has played a crucial role in setting up the Technology Research and Development department, which fundamentally changed the trading landscape in the company. He is one of the main drivers for academic and external collaborations within IMC.

Tongyun Li

Centre for Photonic System Engineering Department
University of Cambridge

2007-2011 PhD student

2012- Now Research Associate

Interests: Digital Radio over Fibre, RF Fronthaul, Radio Access Network, CPRI/NGFI, FPGA based RF designs, Indoor Wireless, small cells and DAS.

Wants: Collaboration with FPGA experts, Ethernet and IP protocol designers, Neutral-host digital RF system designers, optical networking experts.

Vaibhawa Mishra

Università di Roma Tor Vergata

cnit consorzio nazionale interuniversitario per le telecomunicazioni

Valerio Bruschi

Researcher @CNIT

Student in *Ict and Internet Engineering* @University of Rome TorVergata

interests:

- Software Defined Networking
- Enterprise Networks / Network monitoring

I'm currently collaborating with the university in this two European projects:

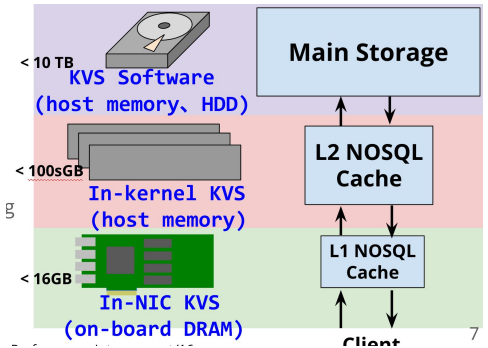
SUPERFLUIDITY

Beba
BEhavioural BAsed forwarding

Yuta Tokusashi @ Keio Univ. Japan

- Introduction
  - A PhD student @ Keio Univ.
  - Visitor @ Univ. of Cambridge
  - JSPS Research Fellow
- Misc
  - Github : github.com/aomtoku
  - Web : aomtoku.github.io
  - Lab : www.arc.ics.keio.ac.jp/english
- Interest
  - An FPGA application
  - Key value store
  - Datacentre networking

- Work in Cambridge
  - Hardware-based flow control
  - Developing large CAM for NetFPGA-SUME
- Previous work
  - Multilevel NOSQL cache architecture (HotI'16)



Today's talk!!

Youngho, Kim

- Samsung Electronics Network Business
- Electrical Engineering at KOREA Univ.
  (Mobile Network & Communications Lab.)

- Has
  - Work experience of network equipment implementation
  - A passion of programmable data plane
- Wants
  - How to use P4 in NetFPGA
  - How to use NetFPGA in P4 research

Zhenyu Wen

I am a research associate in University of Edinburgh. I am involved in the NMaaS (Network Measurement as a Service), working with Myungjin Lee (Edinburgh), Dimitrios Pezaros (Glasgow).

NMaaS aims to design and develop a native network measurement-as-a-service framework that will allow tenants to express their measurement needs and therefore building the corresponding complex service-level performance functions out of simple monitoring primitives.

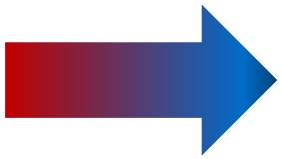
I was a PhD student in Cloud computing with particular focus on optimization the monetary cost of deploying workflow applications over federated Clouds in Newcastle University.

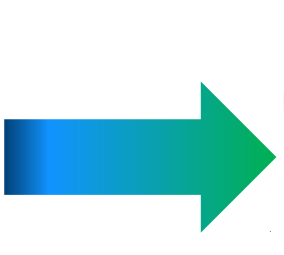
Noa Zilberman

Research Fellow
Computer Laboratory, University of Cambridge

- NetFPGA-SUME Chief Architect
- High Performance Systems:
  - Networking devices
  - Server architectures
  - Rack-scale computing

- Interests: From silicon design to network-wide measurements





- Current Projects/Contributions: CAND, PERF, Gadget, Low latency, Hyper-scale networks, Hybrid networks, EMU, P4->NetFPGA, Huge (T)CAM, ….